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Description

MOSFET PERFORMANCE IMPROVEMENT USING DEFORMATION IN SOI STRUCTURE

Background of Invention

[0001] The invention generally relates to methods for manufacturing a semiconductor device with improved device performance, and more particularly to methods for manufacturing semiconductor devices by imposing tensile and compressive stresses in the substrate.

[0002] Mechanical stresses (e.g., tensile stress and compressive stress) within a semiconductor substrate can modulate device performance, which means stresses within a semiconductor substrate enhance semiconductor device characteristics. Thus, the characteristics of a semiconductor device can be improved by creating tensile and/or compressive stresses in the channel regions of an N type device (e.g., NFET) and/or a P type device (e.g., PFET). However, the same stress component, either tensile or com-

pressive stress, discriminatively affects the characteristics of an N type device and a P type device. For example, when tensile stress is applied to a device in the direction of current flow, the performance of an N type device is enhanced but the performance of a P type device is degraded. Thus, in order to maximize the performance of both N type and P type devices formed on the same semiconductor substrate, each stress component should be selectively engineered and applied to either NFETs or PFETs.

[0003] To selectively create tensile stress to an N type device and compressive stress to a P type device, respectively, distinctive processes and different combinations of materials are used. For example, a trench isolation structure can be used in forming N type and P type devices. When the trench isolation structure is formed, an isolation region for the N type device contains the isolation material which applies appropriate stress to the N type device in a longitudinal direction and in a transverse direction. Further, the first isolation region and the second isolation region are provided for the P type, which apply a unique mechanical stress on the P type device in the longitudinal direction.

[0004] Alternatively, liners can be formed on the side surfaces of

a gate electrode, to selectively induce appropriate stress types in the channels of the N type or P type devices. By providing liners, it is possible to apply appropriate stress closer to the device than relying on the trench isolation fill technique.

[0005] While these methods enables selectively applying tensile stress to the N type device and compressive stress to the PFET device along the longitudinal direction, they require more complicated processing steps and specific materials, thereby increasing manufacturing costs. Further, only a moderate amount of stress is obtained, such as only in the order of hundreds of MPa.

[0006] Therefore, there is a need for more cost-effective and cost-effective methodology for creating larger amount s of tensile and compressive stresses for both N type and P type devices without departing from readily available processing techniques.

Summary of Invention

[0007] In an aspect of the invention, a method for manufacturing a semiconductor device is provided. The method includes forming a semiconductor layer on a substrate. The first region of the substrate is expanded to push up the first portion of the semiconductor layer. The second region of

the substrate is shrunk or compressed to pull down the second portion of the semiconductor layer. An N type device is formed over the first portion of the semiconductor layer. A P type device is formed over the second portion of the semiconductor layer.

[0008] In another aspect of the invention, a method of manufacturing a semiconductor device is provided. A semiconductor layer is formed on a substrate. An expansion element is selectively ion-implanted in the first region of the substrate. A compression element is selectively ion-implanted in the second region of the substrate. Annealing is performed to expand the first region and to shrink or compress the second region. The expanded first portion pushes up the first portion of the semiconductor layer and the compressed second portion pulls down the second portion of the semiconductor layer. An N type device is formed on the first portion of the semiconductor layer. A P type device is formed on the second portion of the semiconductor layer.

[0009] Yet another aspect of the invention is a semiconductor having a substrate comprising an expanded region and a compressed region. A semiconductor layer is formed on the substrate and have the first portion pushed up by the

expanded region and the second portion pulled down by the compressed region. An N type device is formed on the first portion, and a P type device formed on the second portion.

Brief Description of Drawings

[0010] Figure 1 depicts desired tensile and compressive stress for an N type device and a P type device, respectively;

[0011] Figures 2 to 7 depict sequential phases of the method according to an embodiment of the invention; and

[0012] Figure 8 depicts a top view of a semiconductor device shown in Figure 3 after the first mask is removed and the second mask is formed thereon to expose a PMOS region according to an embodiment of the invention.

Detailed Description

[0013] The invention introduces a method for increasing device performances for both an N type device and a P type device, which is easily integrated into conventional processing steps without significantly increasing manufacturing costs. This is achieved by selectively introducing tensile and compressive strains in portions of a semiconductor substrate or layer on which an N type device and a P type device are formed. In general, the tensile strain is intro-

duced by expanding a portion of the substrate or layer for the N type device, and the compressive strain is introduced by compressing a portion of the substrate or layer for the P type device.

[0014] Figure 1 illustrates desired stress types for improving the performance of an N type device (e.g., NFET) and a P type device (e.g., PFET). Each of the NFET and PFET has a source region, a gate region and a drain region, as shown therein. The arrows extending outwardly from the active area illustrate tensile stress, and the arrows extending inwardly towards the PFET device illustrate compressive stress. The arrows outwardly extending from the NFET in both the transverse and longitudinal directions illustrate tensile stress desirable for the NFET. Similarly, the arrows extending inwardly towards the PFET in the longitudinal direction illustrates compressive stress desirable for the PFET. The range of stresses needed to influence device drive currents is of the order of a few hundred MPa to a few GPa. The width and the length of the active area of each device is represented by "W" and "L", respectively.

[0015] Figure 2 shows a substrate structure that is divided into an NMOS region and a PMOS region for illustration purposes. Particularly shown is a silicon-on-insulation (SOI)

type substrate structure. The substrate structure has a semiconductor substrate 10, which is typically a silicon substrate, a buried oxide layer 12 formed on the substrate 10, and a semiconductor layer 14, which is typically a silicon layer, formed on the buried oxide layer 12. Subsequently, as shown in Figure 3, shallow trench isolation (STI) regions 16 are formed in portions of the semiconductor layer 14 to isolate individual device regions from each other.

[0016] As shown in Figure 4, the first mask layer 18 is formed on the substrate structure to selectively expose the device region of the NMOS region while masking the PMOS region. Subsequently, an expansion element (e.g., O_2) is ion-implanted, as shown by arrows "A", onto the exposed surface portion of the semiconductor layer 14 in the NMOS region. The ion-implantation is controllably performed such that the implanted expansion element forms the first region 20 in a portion of the substrate 10 underlying the exposed surface portion. Also, the concentration peak of the implanted expansion element is confined within the first region 20. In an embodiment, the expansion element is ion-implanted at an implantation concentration of approximately 1×10^{14} atoms/cm^2 to 5×10^{16}

atoms/cm^2 and at an implantation energy of approximately 30 KeV to 300 KeV.

[0017] After removing the first mask 18 from the substrate structure, as shown in Figure 5, the second mask 22 is formed thereon to selectively expose the device region of the PMOS region while masking the NMOS region. Subsequently, as shown by arrows "B", a compression element (e.g., He, Ar or other noble gas) is ion-implanted, onto the exposed surface portion of the semiconductor layer 14 in the PMOS region.

[0018] The ion-implantation process is controllably performed such that the implanted compression element forms a second region 24 in a portion of the substrate underlying the exposed surface portion. Also, the concentration peak of the implanted compression element is confined within the second region 24. In an embodiment, the compression element is ion-implanted at an implantation concentration of approximately 1 x 10^{14} atoms/cm^2 to 5 x 10^{16} atoms/cm^2 and at an implantation energy of approximately 30 KeV to 300 KeV.

[0019] Upon forming the first region 20 containing the expansion element and the second region 24 containing the compression element, annealing is performed to activate the

implanted expansion element and the compression element. As shown in Figure 6, when annealing is performed, the first region 20 is activated and the expansion element expands the area that was previously occupied by the first region. This occurs through internal oxidation when the implanted O_2 reacts with the silicon and converts to silicon dioxide with its associated volume expansion. This expansion pushes up the portions of the oxide layer 12 and the semiconductor layer 14 overlying the expanded area, thereby increasing tensile stress in the surface portion of the semiconductor layer 14 overlying the expended area.

[0020] Also, upon annealing, the second region 24 is activated and the compression element shrinks the area which was previously occupied by the second region. This compression pulls down the portions of the oxide layer 12 and the semiconductor layer 14 overlying the compressed area, thereby increasing compressive stress in the surface portion of the semiconductor layer 14 overlying the compressed area. The respective arrows shown in Figure 6 illustrate the regions 22 and 24 being expanding and compressed upon annealing.

[0021] Figure 7 shows gate electrodes 30 formed on the semi-

conductor layer 14 with a gate oxide layer 28 therebetween in the NMOS area and the PMOS area. Although it is not shown here, further processing steps would include forming N type source and drain regions in the NMOS area to constitute an N type device and P type source and drain regions in the PMOS area to constitute a P type device. Since the N type device is formed on the portion of the semiconductor layer 14 that has tensile strain, the performance of the N type device is significantly improved. Also, due to the compressive strain the performance of the P type device is significantly improved.

[0022] Figure 8 shows a top view of the substrate structure shown in Figure 4 prior to ion-implanting the compression element in the PMOS region. The dotted line shows an interface between a device region 32 and the STI region 16 surrounding the device region 32. The second mask 22 covers not only the STI region 16 but also portions of the device region 32 except for a center portion of the device region expected to be a channel region for a PMOS device to be formed.

[0023] Thus, according to an embodiment of the invention, the compression element is ion-implanted to an area of the PMOS device region 32 which is smaller than that of the

NMOS device region because the strain needed in the PMOS region is preferably only longitudinally compressive as seen in Figure 1.

[0024] As explained above, the invention enables improving device performance of both an N type device and a P type device by selectively applying tensile stain in the active area, on which an N type device is formed and selectively applying compressive strain in the active region, on which a P type device is formed.

[0025] The tensile strain is created by expanding a portion of the substrate underlying the N type device. The expanded portion of the substrate pushes up the buried oxide layer and the silicon layer, thereby creating tensile stress to the active region of the silicon layer in the NMOS area. The compressed portion of the substrate pulls down a portion of the substrate underlying the P type device, thereby creating compressive stress to the active region of the silicon layer in the PMOS area.

[0026] The selective application of tensile strain and compressive strain is obtained by using readily available processing steps. Especially, since only two additional photolithography steps are required for the masking steps, the invention achieves significant improvement in device perfor-

mance without significant increase in manufacturing costs.

[0027] While the invention has been described in terms of embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.